Notice of Allowability	Application No.	Applicant(s)	
	09/823,700	MOLSON ET AL.	
	Examiner	Art Unit	
	Kandasamy Thangavelu	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *July 28, 2005*.

2. ☒ The allowed claim(s) is/are *1,3-18,22-26,30,31,34-50,54,57-59 and 61*.

3. ☒ The drawings filed on *30 March 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 6/21/2001
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Clean copy of amended claims*.

DETAILED ACTION

Introduction

1. This communication is in response to the Applicants' communication dated July 28, 2005. Claims 22, 34 and 54 were amended. Claims 1-60 of the application are pending.

Examiner's Amendment

2. Authorization for this examiner's amendment was given in a telephone conversation by Mr. Godfrey Kwan on August 26, 2005.

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicants, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

3. In Claim 1:

Replace claim 1 with:

1. A method for generating operationally limited hardware and software for a programmable device, the method comprising:

identifying license information associated with a protected intellectual property block configured for implementation on the programmable device, wherein the license information identifies a parameter associated with a prototype operation range and a production operation range; and

generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information associated with the intellectual property block.

In Claim 2:

Delete Claim 2.

In Claim 5, Lines 1 to 2, "the number of pin contacts"

has been changed to

-- a number of pin contacts --

In Claim 7, Lines 1 to 2, "the number of input signals"

has been changed to

-- a number of input signals --

In Claim 8, Lines 1 to 2, "the number of output signals"

has been changed to

-- a number of output signals --

In Claim 9, Line 2, "the status of either the hardware or the software"

has been changed to

-- a status of either the hardware or the software --

In Claim 10, Lines 1-2, "the parameter is limited by preselected fabrication"

has been changed to

-- the parameter is set by preselected fabrication --

In Claim 11, Lines 1-2, "the parameter is limited by preselected augmentation"

has been changed to

-- the parameter is set by preselected augmentation --

Replace claim 14 with:

14. The method of Claim 61 further comprising disabling the hardware after the run time has reached the time limit.

In Claim 16, Line 2, "a global tri-state of the hardware IO"

has been changed to

-- a global tri-state of hardware IO --

In Claims 19-21:

Delete Claims 19-21.

In Claim 22:

Replace claim 22 with:

22. A method for disabling a hardware during operation of the hardware, wherein the hardware is a programmable chip configured using a software tool having access to a plurality of intellectual property blocks for implementation on the programmable chip, the method comprising:

identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype operation mode and (ii) too short for use of the hardware in a production operation mode, wherein the run time limit has been set using license information associated with at least one of the plurality of intellectual property blocks;

measuring a time elapsed during operation of the hardware; and

disabling the hardware after the time elapsed reaches the run time limit.

In Claim 23, Line 2, "clock associated with the hardware device"

has been changed to

-- clock associated with the hardware --

In Claim 25, Line 2, "a global tri-state of the hardware I/O"

has been changed to

-- a global tri-state of hardware I/O --

In Claims 27-29:

Delete Claims 27-29.

In Claim 30:

Replace claim 30 with:

30. A programmable chip that can be operationally limited during operation, comprising:

a clock operable to measure a run time;

a memory including a run time limit, the run time limit being (i) long enough to permit testing of the programmable chip in a prototype operation mode and (ii) too short for use of the programmable chip in a production operation mode, wherein the run time limit has been selected at least in part using license information associated with a protected intellectual property block; and

circuitry configured to disable the programmable chip after clock measures that the run time has reached the run time limit.

In Claim 31:

Replace claim 31 with:

31. The programmable chip of Claim 30 wherein the programmable chip is disabled using one of the following:

a reset of a register in the programmable chip,

a global tri-state of I/O of the programmable chip, and

a random failure within the programmable chip.

In Claims 32-33:

Delete Claims 32-33.

In Claim 34:

Replace claim 34 with:

34. A computer program product associated with a computer readable medium including computer code which when executed on a computer performs a process of generating operationally limited hardware and software for a programmable chip, the computer program product comprising:

computer code for identifying a protected intellectual property block associated with a design for implementation on the programmable chip;

computer code for identifying a parameter using license information associated with the protected intellectual property block, wherein the parameter is associated with a first operation range and a second operation range; and

computer code for generating operationally limited hardware and software, wherein the hardware and software are operationally limited based on the parameter identified using license information.

In Claim 37, Line 2, "the number of pin contacts"

has been changed to

-- a number of pin contacts --

In Claim 39, Line 2, "the number of input signals"

has been changed to

-- a number of input signals --

In Claim 40, Line 2, "the number of output signals"

has been changed to

-- a number of output signals --

In Claim 41, Line 2, "the status of either the hardware or the software"

has been changed to

-- a status of either the hardware or the software --

In Claim 42, Lines 1-2, "the parameter is limited by preselected fabrication"

has been changed to

-- the parameter is set by preselected fabrication --

In Claim 43, Lines 1-2, "the parameter is limited by preselected augmentation"

has been changed to

-- the parameter is set by preselected augmentation --

In Claim 46:

Replace claim 46 with:

46. The computer program product of Claim 45 further comprising computer code generating operationally limited hardware and software for disabling the hardware after the run time has reached the run time limit.

In Claim 48, Line 2, "a global tri-state of the hardware IO"

has been changed to

-- a global tri-state of hardware IO --

In Claims 51-53:

Delete Claims 51-53.

In Claim 54:

Replace claim 54 with:

54. A system for generating operationally limited hardware and software for a programmable chip, the system comprising:

means for identifying a protected intellectual property block associated with a design for implementation on the programmable chip;

means for identifying license information associated with the protected intellectual property block, wherein the license information identifies a parameter associated with a first operation range and a second operation range; and

means for generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information.

In Claims 55-56:

Delete Claims 55-56.

In Claim 57:

Replace claim 57 with:

57. The system of Claim 54 wherein the operational parameter is time and further wherein the first operation range is a prototype operation time range and the second operation range is a production operation time range.

In Claim 58:

Replace claim 58 with:

58. The system of Claim 57 wherein the prototype operation time range has a maximum and further wherein the production operation time range has no maximum.

In Claim 60:

Delete Claim 60.

Insert claim 61 as follows:

61. The method of claim 1 further comprising:

operating the hardware and the software in a prototype operation mode and in a production operation mode;

operationally limiting the hardware and the software in the prototype operation mode.

A clean copy of the amended claims is attached.

Reasons for Allowance

4. Claims 1, 3-18, 22-26, 30-31, 34-50, 54, 57-59 and 61 of the application are allowed over prior art of record.

5. The following is an Examiner's statement of reasons for the indication of allowable subject matter:

The closest prior art of record shows:

(1) protecting data by controlling access to data using rules concerning access rights; a method of distributing data for controlled use, by protecting portions of data; access to protected portions of data other than in non-usable form is prevented; intellectual property can be embodied in forms which can be copied from the owner, while the owner still retains the

original; intellectual property is protected using cryptography; once access is granted, it cannot be controlled in any other ways; it is difficult to control copying and secondary distribution and receive payment for all uses; when the data represents computer software, the method controls how much of the software's functionality is available; the degree of protection will depend on the nature of the hardware and the user environment; permitting a user access to the data only in accordance with the rules (**Schneck et al.,** U.S. Patent Application 2001/0021926);

(2) LSI incorporating a plurality of functional blocks developed by different manufacturers; a decryption key disclosed by license to the end user who is using the functional block developed by another company within the system LSI; among the users of this system LSI, only the end users who possess the decryption key can use this functional block; to use the functional block , it is necessary to obtain the decryption key by license from the manufacturer, thus simplifying the management of intellectual property rights (**Amano et al.,** U.S. Patent 6,557,020);

(3) system and method for electronic rights protection by making information to be accessed and used only in authorized ways; a virtual distribution environment (VDE) enforces a secure chain of handling and control to meter, monitor and control use of electronically stored and disseminated information, to protect the rights of various participants in electronic commerce; this ensures proper compensation to the content providers for use of the electronic information; a number of limited rights protection mechanisms protect the rights of the content providers; authorization passwords, protocols, license servers, lock/unlock mechanisms, distribution methods and non-electronic contractual limitations are imposed on the users; VDE allows owners and distributors of electronic information to reliably bill, securely control, audit

and budget the use of commercial information products (**Ginter et al.,** U.S. Patent 5,892,900); and

(4) utilization of parametrizable intellectual property (IP) cores to rapidly develop circuit layouts; techniques using a hierarchical library of silicon IP cores for implementing complex algorithms; the IP cores ensure highly competitive silicon designs in terms of layout, performance and power consumption (**Lightbody et al.,** "Rapid design of a single chip adaptive beamformer", IEEE 1998).

None of these references taken either alone or in combination with the prior art of record discloses a method for generating operationally limited hardware and software for a programmable device, specifically including:

"identifying license information associated with a protected intellectual property block configured for implementation on the programmable device, wherein the license information identifies a parameter associated with a prototype operation range and a production operation range; and

generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information associated with the intellectual property block".

None of these references taken either alone or in combination with the prior art of record discloses a method for disabling a hardware during operation of the hardware, wherein the hardware is a programmable chip, specifically including:

"identifying a run time limit that is (i) long enough to permit testing of the hardware in a prototype operation mode and (ii) too short for use of the hardware in a production operation mode, wherein the run time limit has been set using license information associated with at least one of the plurality of intellectual property blocks;

measuring a time elapsed during operation of the hardware; and

disabling the hardware after the time elapsed reaches the run time limit".

None of these references taken either alone or in combination with the prior art of record discloses a programmable chip that can be operationally limited during operation, specifically including:

"a memory including a run time limit, the run time limit being (i) long enough to permit testing of the programmable chip in a prototype operation mode and (ii) too short for use of the programmable chip in a production operation mode, wherein the run time limit has been selected at least in part using license information associated with a protected intellectual property block; and

circuitry configured to disable the programmable chip after clock measures that the run time has reached the run time limit".

None of these references taken either alone or in combination with the prior art of record discloses a computer program product associated with a computer readable medium including computer code which when executed on a computer performs a process of generating operationally limited hardware and software for a programmable chip, specifically including:

"computer code for identifying a parameter using license information associated with the protected intellectual property block, wherein the parameter is associated with a first operation range and a second operation range; and

computer code for generating operationally limited hardware and software, wherein the hardware and software are operationally limited based on the parameter identified using license information".

None of these references taken either alone or in combination with the prior art of record discloses a system for generating operationally limited hardware and software for a programmable chip, specifically including:

"means for identifying license information associated with the protected intellectual property block, wherein the license information identifies a parameter associated with a first operation range and a second operation range; and

means for generating operationally limited hardware and software, wherein the hardware and software are operationally limited using the parameter identified in the license information".

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Kandasamy Thangavelu whose telephone number is 571-272-3717. The examiner can normally be reached on Monday through Friday from 8:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard, can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to TC 2100 Group receptionist: 571-272-2100.

K. Thangavelu
Art Unit 2123
August 26, 2005

Paul L. Rodriguez 9/1/05
Primary Examiner
Art Unit 2125